FPGA-Based Power Models for Early System-Level Power Estimation

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Theme/Task: 1633.001

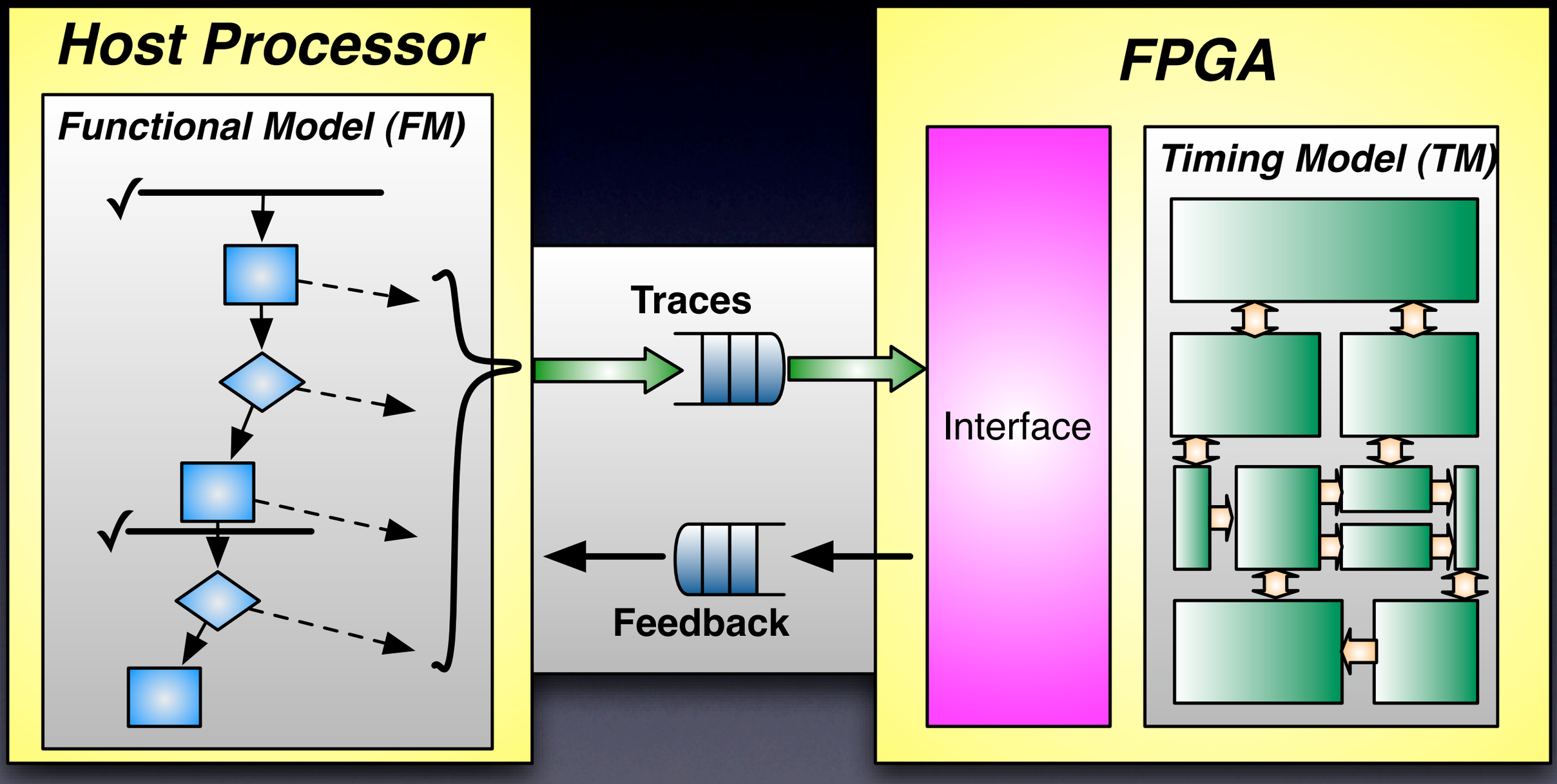
Power

- Power consumption is a key factor in modern processor design
- Architectural design decisions make great impact on power
  - Need better models to make better decisions!
- ***The Dilemma:***
  - Architectural-level: Wattch, SimplePower, etc.
    - Still inaccurate
  - RTL/Gate-level: PowerTheater, Cadence RC, etc.
    - Requires full design
    - Can be very slow

FAST [ICCAD2007, MICRO2007]

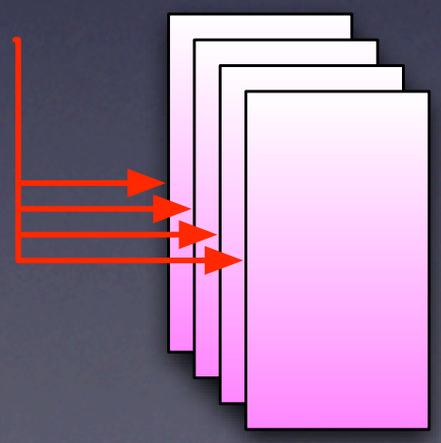
- FPGA-Accelerated Simulation Technology (FAST)
- Partition simulator into:
  - Functional Model (FM)
    - simulates ISA, peripheral functionality
  - Timing Model (TM)
    - simulates timing, details of microarchitecture
- Place TM on hardware!
- Runs significantly **faster** without losing accuracy

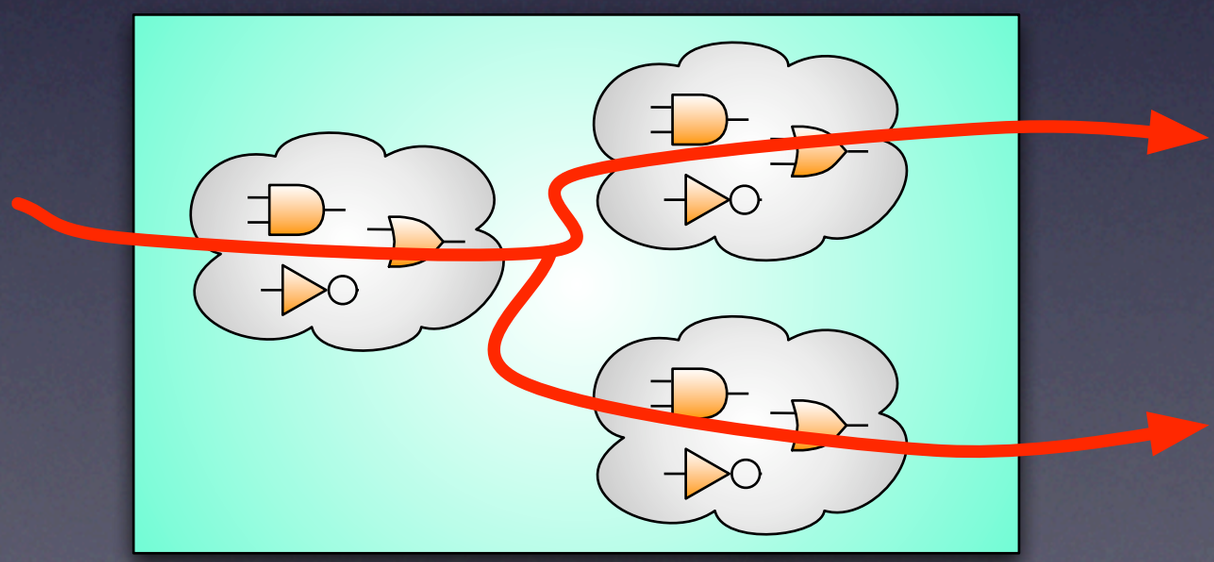
FAST Bird's-eye view



Power Models for FAST

- Identify ***key contributor signals*** to power consumption and create models based on them
- *"Architectural Signals"*
  - *Available* at high-level
    - Cache hit/miss signals, RegFile write data
  - Have more impact on power as they ***drive more logic*** and have ***larger fan-out***





Experiments

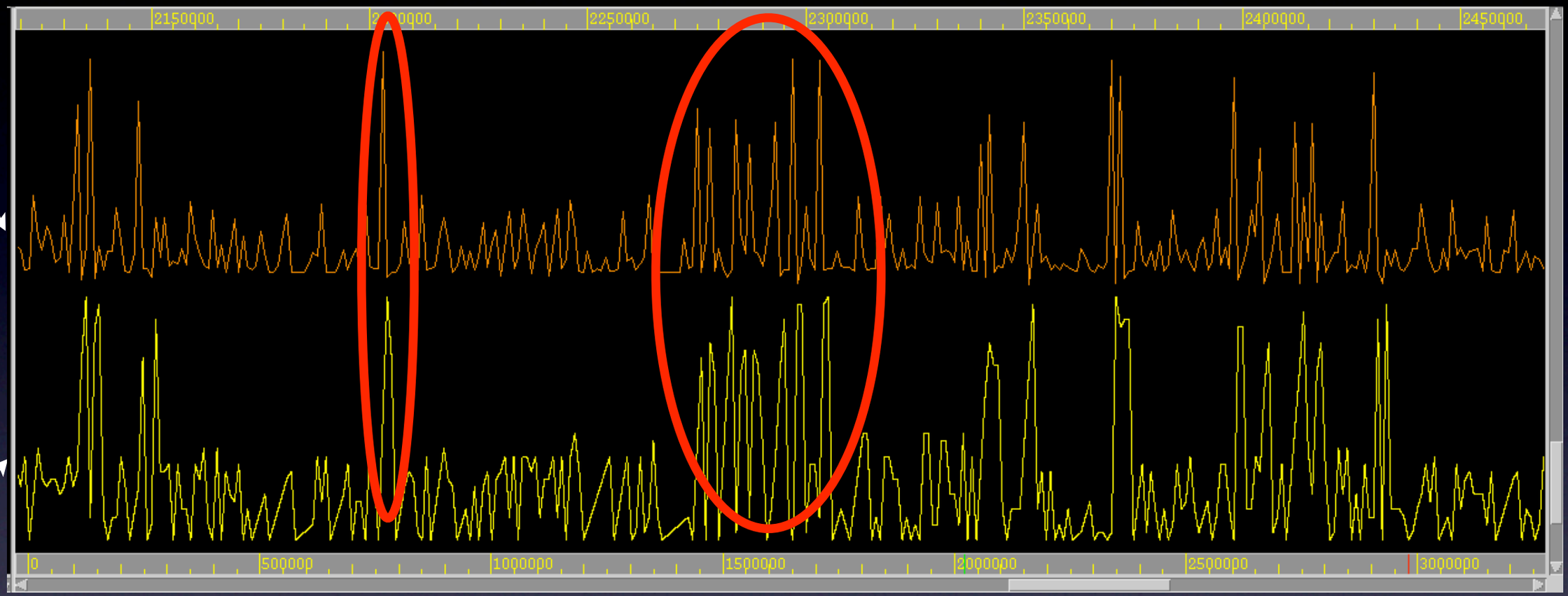
- Applied proposed approach to Freescale z650 embedded processor
  - 32-bit Power ISA
  - 7-stage in-order pipeline
  - 32KB Unified L1 cache (8-way)
  - MMU
- Run PowerTheater on entire RTL

Example (Caches)

- Only used "*Sum of Cache Bank Enable signals*"
- Cache Reads: Access all ways in a set-associative cache
- Cache Writes: Access specific way only

Example (Reg File)

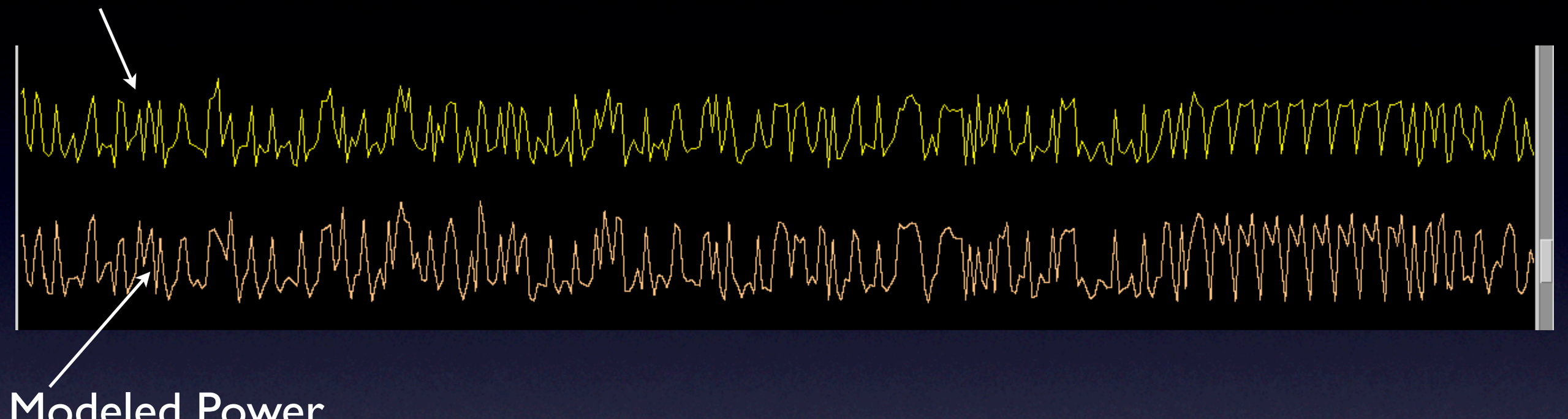
PowerTheater



Modeled Power

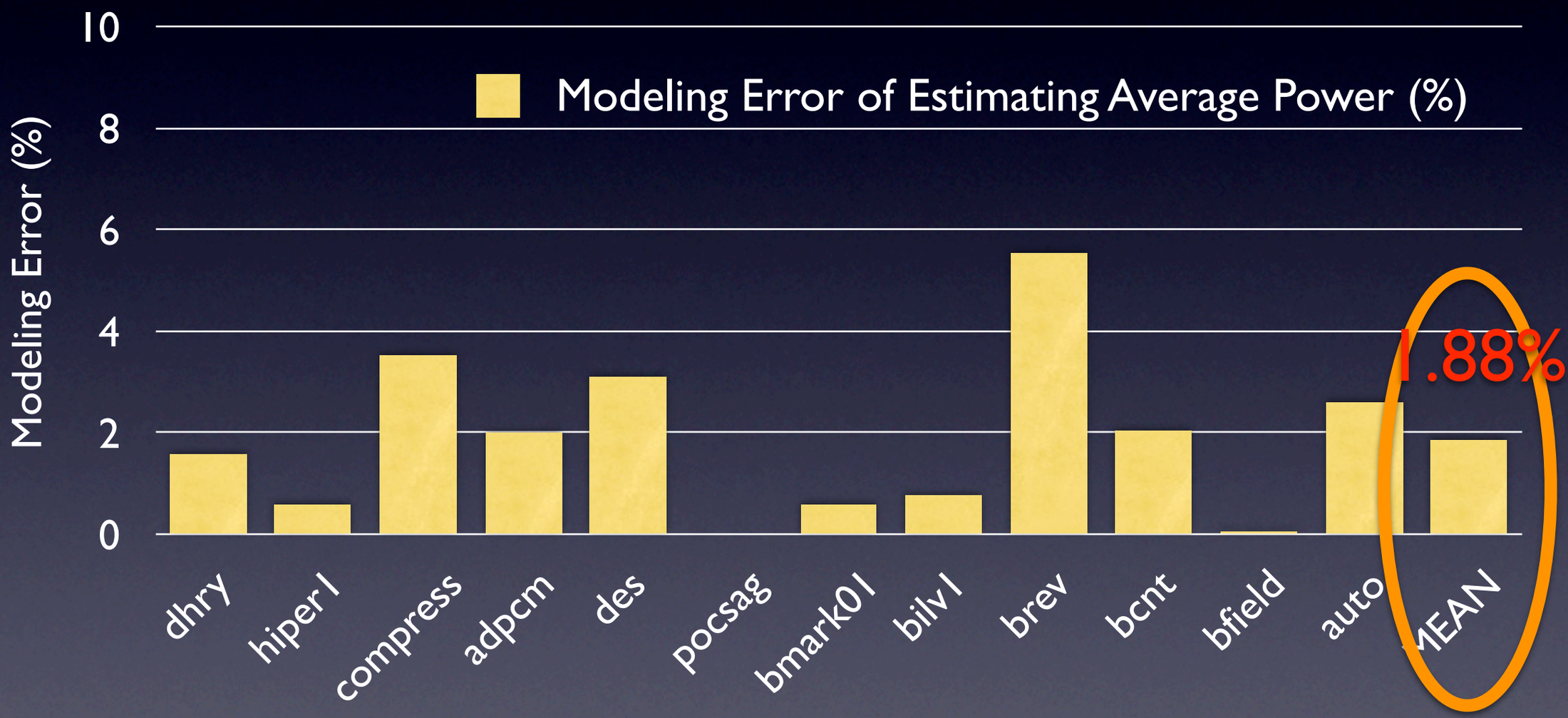
- Only used "*Hamming Distance of Reg File Write Data*"
- The spikes in power indicate more bits have flipped, resulting in more power consumption

Total Power (z650 core)



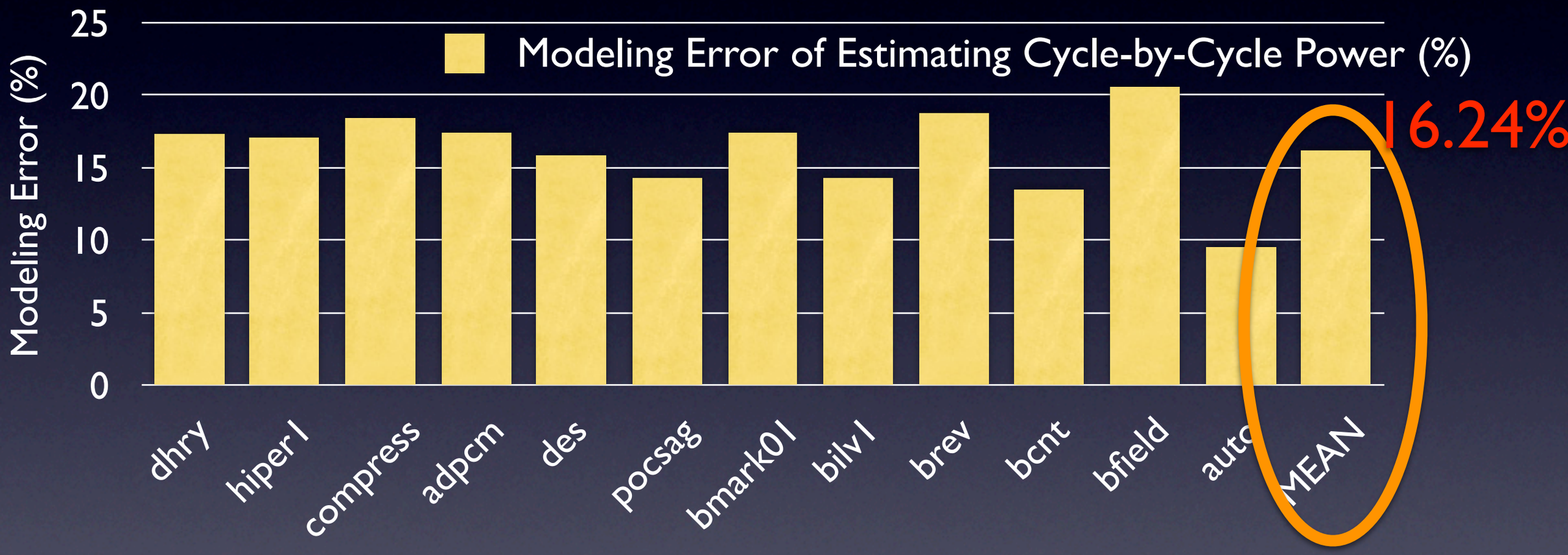
- Only used Cache / Register File signals
  - All other modules are lumped as constant
  - Linear model (aX+bY+c)
- Modeled power tracks PowerTheater fairly accurately

Results (Average Power)



- **Less than 2% off** of RTL PowerTheater estimation

Results (Cycle-by-Cycle Power)

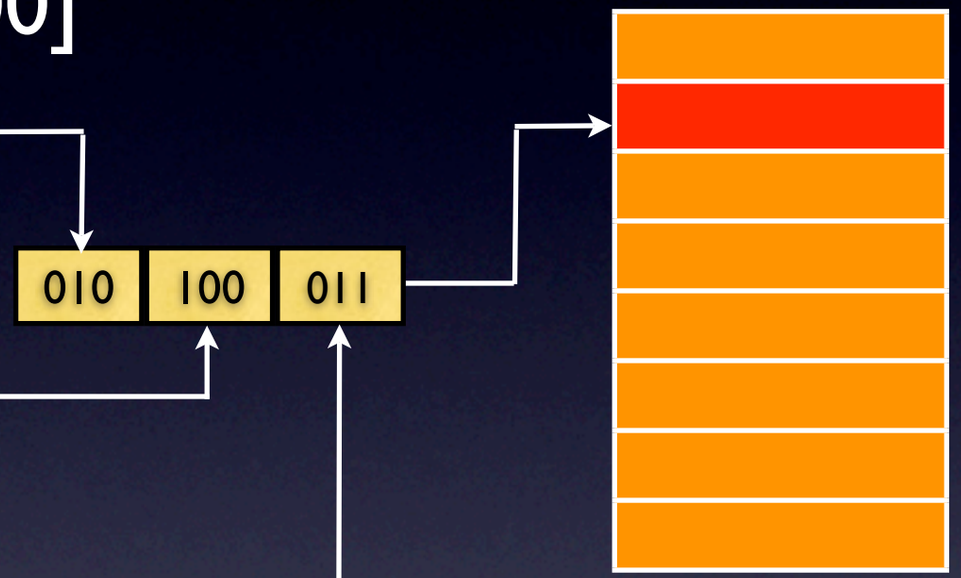


- Measured as *RMS average* of difference between PowerTheater and Modeled power

- **Less than 20% off!**

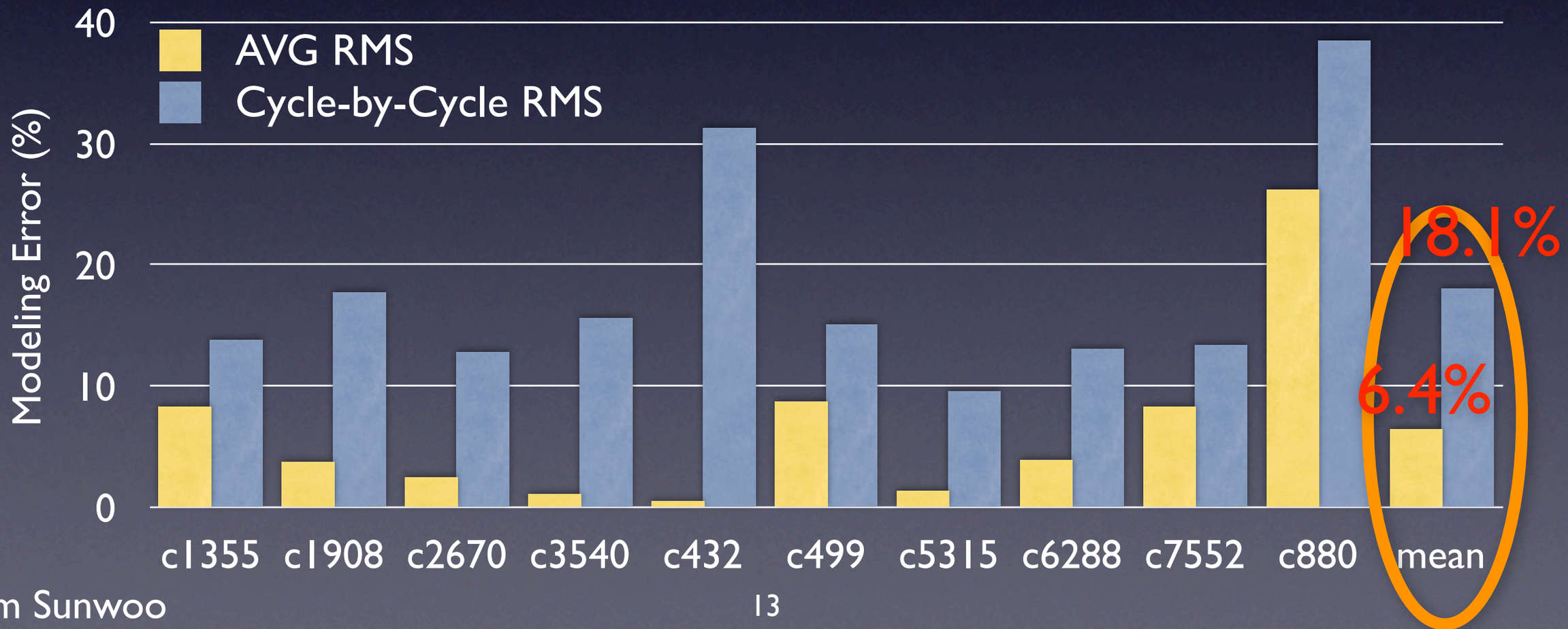
What about other *irregular* logic?

- Macromodeling [GuptaTVLSI2000]
  - Avg Input Signal Probability
    - How many ones?
  - Avg Input Transition Density
    - How many bits flip?
  - Avg Input Spatial Correlation Coeff
    - How close are the ones?
- Look-up Table populated using carefully crafted input vectors
  - Markov Chain Sequence Generator [LiuICCAD2002]
  - Generate 2000 vectors per LUT entry



Macromodeling Results

- ISCAS-85 Benchmark circuits (ALUs, etc.)
- Compared against Synopsys PrimeTime estimates
  - TSMC 130nm library
- Cycle-by-Cycle power modeled within ***20%!***



Integration with Architectural Simulators

- Can use any architectural simulator
  - Power models only use signals that are available at high-level
  - Runs significantly faster than RTL simulation
- FPGA-Accelerated Simulation Technologies (FAST) Simulators
  - Power Models very suitable for FPGAs
    - Virtually no overhead on simulation performance
  - Even faster! (10 MIPS?)

Conclusion

- High-level Power Models
  - Can model average power very accurately (<2%)
  - Can model cycle-by-cycle power at reasonable accuracy (<20%)
  - Can run significantly faster than RTL tools
- Useful to not only hardware designers but also to software developers

Tech Transfer

- Industrial Liaisons
  - James C. Holt (Freescale)
  - Carl E. Lemonds (AMD)
  - Peng Yang (Freescale)
- Internships
  - IBM Austin Research Lab (2006)
  - Freescale (2008)
- Publications
  - ICCAD 2007, MICRO 2007, MTV 2007

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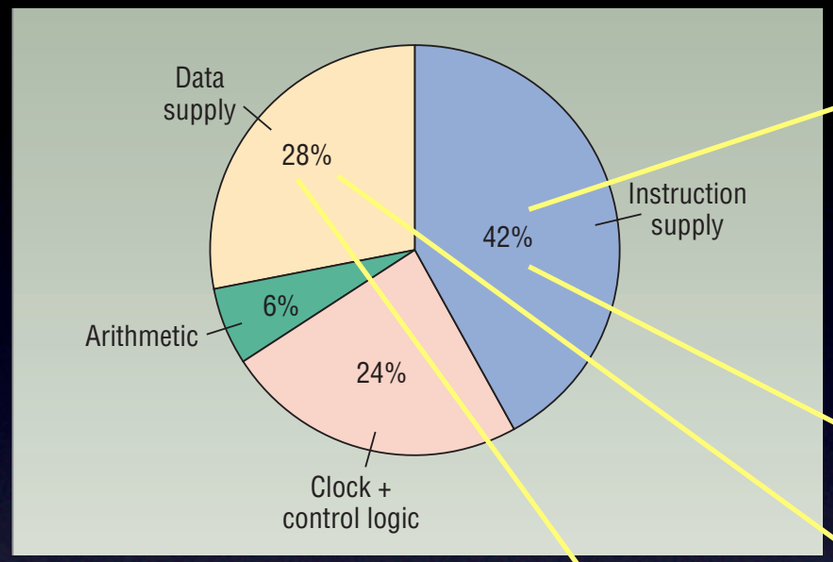
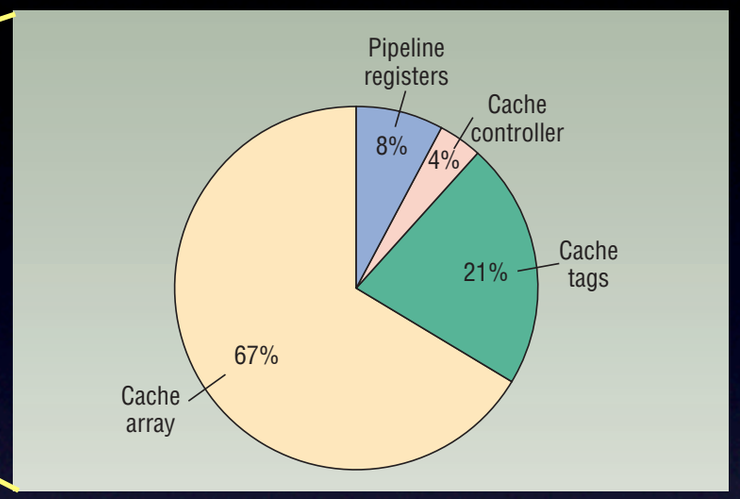
Thank you!

- Questions?

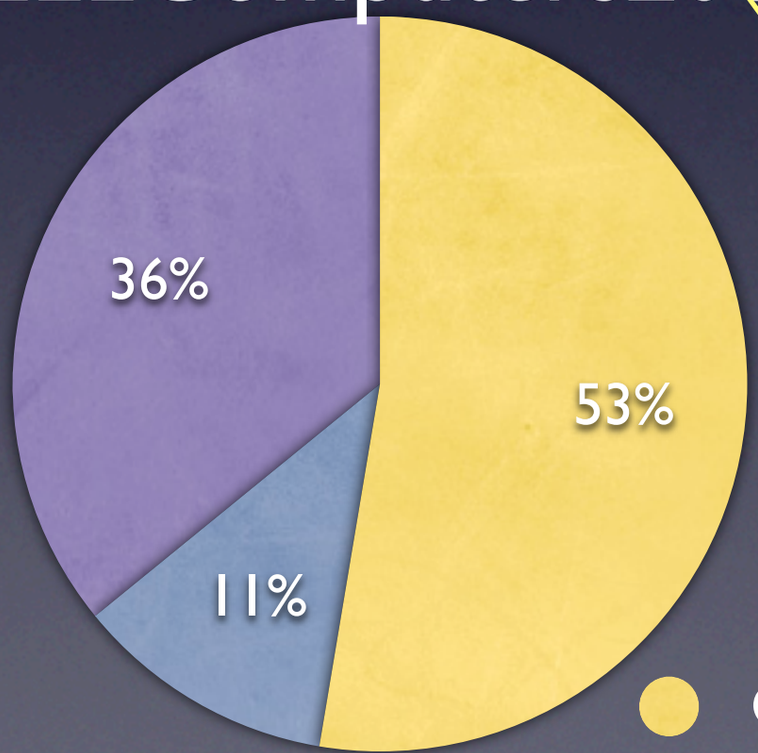
Backup Slides

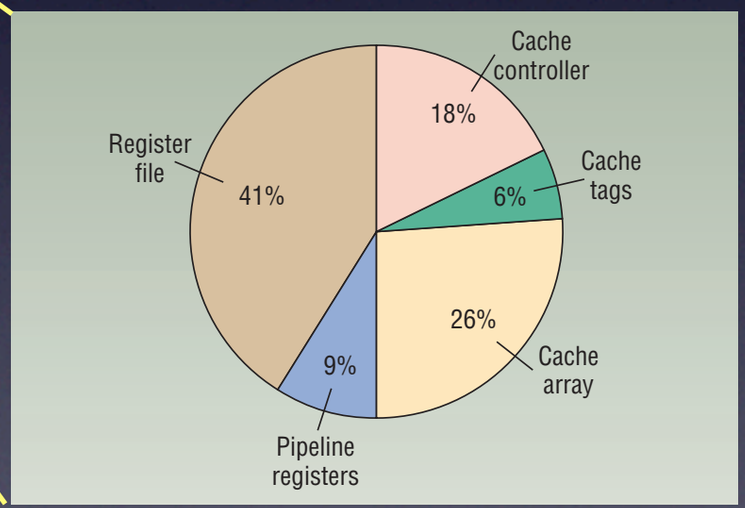
Power Breakdown





Stanford ELM processor [DallyIEEEComputers2008]





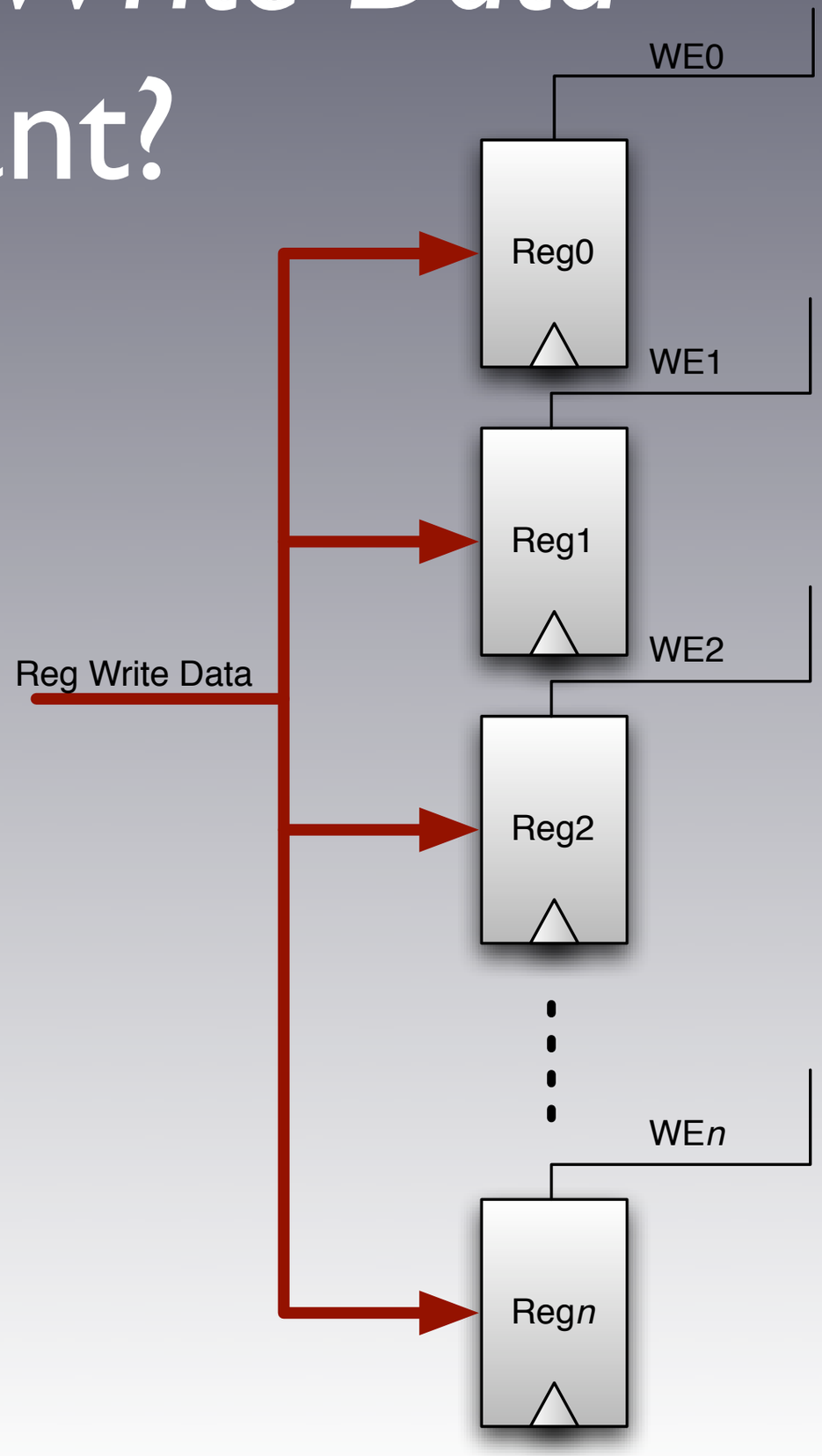
Cache RegFile Others

Why is "*Reg File Write Data*" important?

- Write Data is broadcast

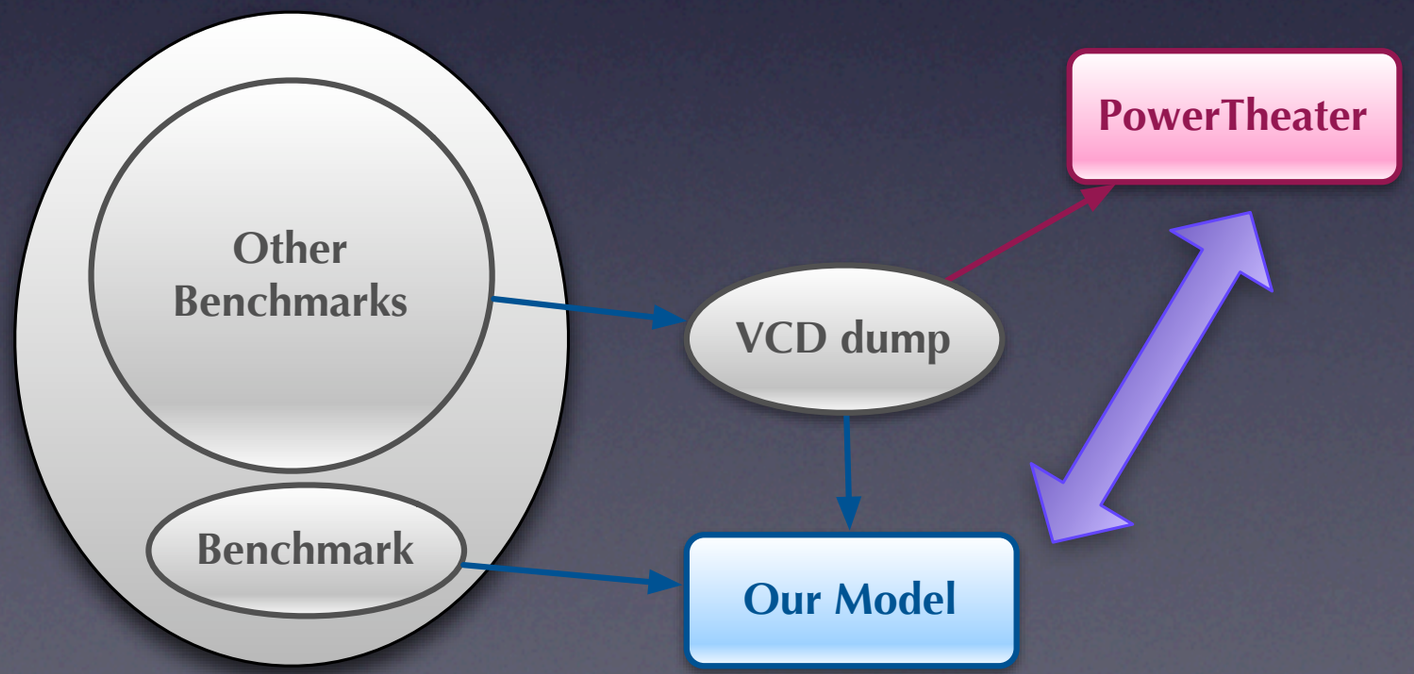
- Although only one register is "*write-enabled*", switching still occurs at all register inputs

- Write Data is globally routed



Benchmarks

- Profiled power model using one benchmark
- Ran 12 different benchmarks from standard benchmark suites
  - Dhrystone, Hiperstone, etc.
  - Sampled 10,000ns from VCD dump
  - Simulating 10,000ns in PowerTheater takes around 4 hours



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Modeling Flow